UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,319	08/17/2001	Gerard Chauvel	TI-31357	5661

23494 7590 09/29/2003

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER
BRAGDON, REGINALD GLENWOOD

ART UNIT	PAPER NUMBER
2188	8

DATE MAILED: 09/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PR4

Office Action Summary	Application No.	Applicant(s)	
	09/932,319	CHAUVEL, GERARD	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-6, 9, 11, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Bausch (6.339,816).

As per claim 1, Bausch teaches a data processing system including a translation look-aside buffer or TLB. Several tasks can share program code ("executing a plurality of program tasks within the processor"). See column 1, lines 43-45. "[Initiating] a plurality of memory access requests in response to the plurality of program tasks" is generally described throughout the patent, noting in particular the execution of write accesses described in columns 1 and 2. The TLB ("caching a plurality...") is described in general in column 1, lines 11-19, noting in particular that Bausch teaches that control information is also stored in the TLB. The system includes an address space identifier (ASID), which identifies a task ("incorporating a task

identification..."). See column 2, lines 1-3 and column 3, lines 6-7. A control bit GL ("shared indicator") is maintained, which indicates if a page globally used (i.e. shared by plural tasks). See column 2, lines 46-47. Bausch teaches that if the GL control bit is set, then all entries in the TLB which relate to global user pages must be declared invalid ("invalidating a portion...that is qualified by the shared indicator"). See column 3, lines 1-3. Bausch teaches that if control bit GL is set, then all entries that relate to global user pages must be declared invalid. See column 3, lines 1-3. A single command would be used to generate this invalidation process.

As per claim 2, Bausch teaches invalidating entries if the GL bit is set (or "shared"). See column 3, lines 1-3.

As per claim 3, Bausch teaches invalidating entries if the GL bit is not set (or "not shared"). See column 3, lines 4-5.

As per claims 5-6, Bausch teaches invalidating entries if the GL bit is not set and based on an ASID ("task identification value"). See column 3, lines 5-11. The ASID represents the "second qualifier value" in claim 6.

As per claim 9, Bausch teaches that the invention therein is contemplated within the MIPS RM4000 environment. The maintaining of access control bits (such as the control bit GL) in a page table entry is an inherent feature of the MIPS RM4000. As evidence thereof, reference is made to the "MIPS R4000 User's Manual, 2nd Edition" where on page 129, under "Servicing", it is taught that physical page frame and access control bits are loaded on a TLB miss.

As per claim 11, Bausch teaches that the invention therein is contemplated within the MIPS RM4000 environment. The maintaining of separate entries in the TLB for multiple tasks for the same virtual address is an inherent feature of the MIPS RM4000. As evidence thereof,

reference is made to the "MIPS R4000 User's Manual, 2nd Edition" where on page 82 it is described for the ASID value that each process (i.e. task) has a distinct mapping of otherwise identical virtual page numbers.

As per claim 14, Bausch teaches a data processing system including a translation look-aside buffer or TLB ("storage circuitry"), which stores pairs of virtual and real addresses and control information. See column 1, lines 11-19. The TLB includes a control bit GL ("shared indicator"), which indicates if a page globally used (i.e. shared by plural tasks). See column 2, lines 46-47. The TLB inherently includes inputs and outputs. Bausch teaches that if the GL control bit is set, then all entries in the TLB which relate to global user pages must be declared invalid ("control circuitry...invalidate...according to the shared indicator"). See column 3, lines 1-3. Bausch teaches that if control bit GL is set, then all entries that relate to global user pages must be declared invalid. See column 3, lines 1-3. A single command would be used to generate this invalidation process.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch in view of Slater, "A Guide to RISC Microprocessors".

As per claims 4 and 15, Bausch does not teach that the system has several levels of TLB and invalidating encompasses invalidating all of the levels of TLB. It is noted that the system of Bausch operates within the context of the MIPS RM4000 system. Slater teaches that it was known within the MIPS R6000 system to include a "2nd" level of TLB, called the TLB slice, in addition to the traditional full TLB. See page 115. Slater also teaches that the TLB slice is updated along with the full TLB. See page 116, second full paragraph. It would have been obvious to one of ordinary skill in the art to have modified the system of Bausch to include a TLB slice as a second level of TLB, because Slater teaches that such an implementation would reduce the amount of transistors on the CPU chip.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch in view of Chaco (6,009,333).

As per claim 16, Bausch does not teach that the system set forth in Bausch is implemented within a personal digital assistant (PDA) Chaco teaches that it was known within the art to implement a PDA using a MIPS R4000 (which is the type of system contemplated by Bausch). It would have been obvious to one of ordinary skill in the art to utilized the system of Bausch within a PDA, as taught by Chaco at column 7, lines 53-58, because such a system would provide a versatile PDA embodiment.

7. Claims 7, 10, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bausch.

As per claim 7, Bausch does not teach that the second qualifier is a processor identifier, utilized in a system with a plurality of processors. However it would have been obvious to one of ordinary skill in the art to have utilized the system of Bausch in a multiprocessor system,

where a processor ID is added to the TLB control information, because multiprocessor systems provide improved processing capability by permitting even greater multitasking and parallel processing.

As per claim 10, Bausch does not teach not storing the control bit GL in the page translation tables. However it would have been obvious to one of ordinary skill in the art to have not included the control bit GL in the page translation tables because the status of a particular entry as being related to multiple tasks may change dynamically, and not storing information that may change quickly within the page tables would save memory, thereby reducing system cost.

As per claims 12-13, Bausch does not teach storing only one entry in the TLB for a particular virtual address regardless of the number of tasks using the entry. However it would have been obvious to one of ordinary skill in the art to have modified Bausch such that only one entry was stored in the TLB for a virtual address regardless of the number of tasks that may access the virtual address associated with that entry, because this would save space in the TLB, allowing more distinct virtual addresses to be stored in the TLB.

Response to Arguments

8. Applicant's arguments filed 19 August 2003 have been fully considered but they are not persuasive.

Applicant argues, with respect to claims 1 and 14, that Bausch does not teach a single command issued from the processor to invalidate TLB entries. The Examiner disagrees.

First, the MIPS R4000 Microprocessor User's Manual teaches processor invalid requests. A processor invalidate request would represent a "single command" from the processor to invalidate an entry. See page 271-273 of the MIPS R4000 Microprocessor User's Manual.

Second, Bausch teaches a valid bit, V, which indicates whether an entry in the TLB is valid or not. The actual act of "invalidating" an entry is nothing more than an operation/command instructing the TLB to mark the valid bit "invalid".

Applicant has argued that in order to invalidate an entry in the MIPS R4000 system, one must read each entry of the TLB through the TLBR instruction, check the G bit or the ASID field, and invalidate the line through a write entry with index according to the need. However, these series of "steps" set forth by Applicant as the process of "invalidating an entry" in the MIPS R4000 TLB goes beyond the claimed "invalidating" set forth in claims 1 and 14. The actual claimed "invalidating" would only correspond to the "step" of "[invalidating] the line through a write entry with index" since it is only this operation that would result in invalidating an entry in the TLB.

Applicant's remarks concerning claim 5 are noted, however they are not persuasive since the Examiner has not referred to the TL bit and modifying the ASID in rejecting claim 5.

Applicant's remarks concerning claim 7 are noted, however they are not persuasive since, although a multiprocessor system may tend to have a separate TLB associated with each processor, this point alone does not teach away from storing a processor ID in the TLB.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)

or

(703) 746-7239 (Official Communications)

(703) 746-7240 (For Status inquiries, draft communications)

and/or

(703) 746-5693 (Use this FAX#, only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal page/amendment be faxed directly to them on occasion).

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
September 20, 2003